Docket No.: M&N-IT-466

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ERIC LIAU

Filed : CONCURRENTLY HEREWITH

Title : METHOD OF GENERATING A TEST PATTERN FOR SIMULATING AND/OR TESTING THE LAYOUT OF AN INTEGRATED CIRCUIT

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Hsiao, M. S. et al.: "Sequential Circuit Test Generation Using Dynamic State Traversal", European Design and Test Conference, March 1997, pp. 22-28;

Singer, S. et al.: "Virtual Test Automation Generator (VTAG)", Navair Lakehurst, May 5, 2000, pp. 1-10;

Rudnick, E. M. et al.: "Automatic Test Generation", "Genetic Algorithms for VLSI Design, Layout and Test Automation", Prentice Hall, Upper Saddle River, NY, 1999, pp. 159-166 and pp. 179-184.

Respectfully submitted,

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For Applicant

Date: July 18, 2003

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FORM PTO-1449 (SUBSTITUTE) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Attorney Docket No.: M&N-IT-466 Appl. No.: Applicant: ERIC LIAU Filing Date: July 18, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	TRANSL. NO
	J							
	K							
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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